

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A stacked semiconductor device consisting of a first semiconductor device having outside electrode terminals on a [[its]] lower surface thereof, a second semiconductor device electrically connected with said first semiconductor device and secured on said first semiconductor device, characterized in that[[::]] said first semiconductor device [[has]] comprising:

a first semiconductor substrate;

first circuit elements at a first main surface of said first semiconductor substrate;

a first multilayer wiring part on said first including a plurality of circuit elements and configured of a first formed at a first main surface side of said semiconductor substrate and wiring electrically connected with said first circuit elements and a first insulating material layer, the first wiring and the first insulating material layer being stacked alternately with the first insulating material layer being an uppermost layer;

a first insulating layer for covering said first insulating material layer of said first multilayer wiring part and provided all over said first semiconductor substrate, said first insulating layer is a support member of said first semiconductor substrate;

a second insulating layer for covering a second main surface of said first semiconductor substrate that is to become an opposite face against the first main surface of said first semiconductor substrate;

a plurality of first post electrodes formed on respective-specified said first wiring of said first multilayer wiring part [[to be]] and each having a top surface and side surfaces, the top surfaces of said first post electrodes exposed from [[in]] a surface of said first insulating layer and all the side surfaces of said first post electrodes covered by said first insulating layer;

a plurality of first through-type electrodes provided to pierce penetrating from a specified depth of said first multilayer wiring part to a surface of said second insulating layer through said first semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, said first through-type electrodes insulating from brought into contact to said first semiconductor substrate through an by a first insulating film and connected with said first specified wiring of said first multilayer wiring part respectively; and

said outside electrode terminals connected to said first through-type electrodes[[;]].

said second semiconductor device comprising [[has:]]
a second semiconductor substrate;
second circuit elements formed at a first main surface of said second semiconductor substrate;

a second multilayer wiring part on said second including a plurality of circuit elements and configured of a second formed at a first main surface side of said semiconductor substrate and wiring electrically connected with said second circuit elements and a second insulating material layer, the second wiring and the second insulating material layer being stacked alternately with the second insulating material layer being an uppermost layer;

a third [[first]] insulating layer for covering said second insulating material layer of said second multilayer wiring part and provided all over said second semiconductor substrate, said third insulating layer is a support member of said second semiconductor substrate;

a fourth second insulating layer for covering a second main surface of said second semiconductor substrate that is to become an opposite face against the first main surface of said second semiconductor substrate; and

at least second post electrodes formed on said second respective specified wiring of said second multilayer wiring part [[to be]] and each having a top surface and side surfaces, the top surfaces of said second post electrodes exposed [[in]] from a surface of said third [[first]] insulating layer and all the side surfaces of the second post electrodes covered by said third insulating layer, or a plurality of second through-type electrodes penetrating from a specified depth of said second multilayer wiring part to a surface of said fourth insulating layer provided to pierce through said second semiconductor substrate and said second insulating layer from specified depth of said

multilayer wiring part, said second through-type electrodes insulated from brought into contact to said second semiconductor substrate through an by a second insulating film and connected with said second specified wiring of said second multilayer wiring part respectively, [[and]]

in said first semiconductor device, said first post electrodes or said first through-type electrodes are at the come in a lower surface thereof and said post-electrodes or said through-type electrodes in the lower surface are provided with said outside electrode terminals[[;]], and

said second through-type electrodes or said second post electrodes at a in the lower surface of said second semiconductor device are electrically connected with said first post electrodes or said first through-type electrodes in the at an upper surface of said first semiconductor device through joints.

Claim 2 (Currently Amended): The stacked semiconductor device according to claim 1, having a third semiconductor device stacked and secured between said first semiconductor device and said second semiconductor device, wherein ever one to a plurality of steps, characterized in that[[;]] said third semiconductor device comprises [[has]]:

a third semiconductor substrate;
third circuit elements at a first main surface of said third semiconductor substrate;

a third multilayer wiring part including a plurality of on said third circuit elements and configured of a third formed at a first main surface side of said semiconductor substrate and wiring electrically connected with said third circuit elements and a third insulating material layer, the third wiring and the third insulating material layer being stacked alternately with the third insulating material layer being an uppermost layer;

a fifth [[first]] insulating layer for covering said third insulating material layer of said third multilayer wiring part and provided all over said third semiconductor substrate, said fifth insulating layer is a support member of said third semiconductor substrate;

a sixth second insulating layer for covering a second main surface of said third semiconductor substrate that is to become an opposite face against the first main surface of said third semiconductor substrate;

a plurality of third post electrodes formed on said third respective specified wiring of said third multilayer wiring part [[to be]] and each having a top surface and side surfaces, the top surfaces of said third post electrodes exposed [[in]] from a surface of said [[first]] fifth insulating layer and all the side surfaces of said third post electrodes covered by said fifth insulating layer;

a plurality of third through-type electrodes provided to pierce penetrating from a specified depth of said third multilayer wiring part to a surface of said sixth insulating layer through said third semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, said third through-type electrodes insulated from brought into contact to said third semiconductor substrate through an by

a third insulating film and connected with said third specified wiring of said third multilayer wiring part respectively, and

the third post electrodes or the third through-type electrodes on [[the]] upper/lower surfaces of said third semiconductor device are electrically connected with the first post electrodes or the first through-type electrodes of the first semiconductor device at [[the]] an upper stage side and the second semiconductor device at [[the]] a lower stage side through joints.

Claim 3 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second semiconductor devices are disposed as at the respective stages will become a single body, have a same size, and the respective semiconductor devices overlap each other in corresponding fashion in a same size.

Claim 4 (Currently Amended): The stacked semiconductor device according to claim 1, comprising characterized in that a plurality of said second semiconductor devices that are smaller than said first semiconductor device, and are disposed and secured in parallel on said first semiconductor device.

Claim 5 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that the respective first through-type electrodes or the first

respective post electrodes on the at an upper surface of said first semiconductor device and the respective second through-type electrodes or the second respective post electrodes at a on the lower surface of said second semiconductor device are brought into correspondence and are electrically connected respectively through said joints.

Claim 6 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said joints are not used for joining the respective through-type electrodes or the respective post electrodes on the upper surface of said first semiconductor device with the respective through-type electrodes or the respective post electrodes on the lower surface of said second semiconductor device but, said post electrodes or said through-type electrodes engaged in said joining of said one semiconductor device protrude and those protruding portions are connected to said post electrodes or said through-type electrodes of the facing semiconductor device with comprise metal joining.

Claim 7 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second post electrodes are formed of comprise a plating film, stud bump electrodes or a CVD film.

Claim 8 (Currently Amended): The stacked semiconductor device according to claim 1, further comprising characterized in that a metal plate having insulating holes is present

and disposed between said first semiconductor device and said second semiconductor device,

wherein in [[the]] a portion of said insulating holes, first ones of said first through-type electrodes or said first post electrodes on the at an upper surface of said first semiconductor device are electrically connected with first ones of said second through-type electrodes or said second post electrodes at a on the lower surface of said second semiconductor device through said joints in a state without contacting said metal plate, and second ones of said first through-type electrodes and said first post electrodes of said first semiconductor device and second ones of said second through-type electrodes and said second post electrodes of said second semiconductor device [[to]] that face said metal plate are electrically connected with said metal plate through said joints.

Claim 9 (Currently Amended): The stacked semiconductor device according to claim 8, wherein the second ones of characterized in that said first and second through-type electrodes or said first and second post electrodes to be given are provided with a power supply potential of said semiconductor device or a ground potential are connected with through said metal plate.

Claim 10 (Currently Amended): The stacked semiconductor device according to claim 1, wherein one characterized in that out of said first and second semiconductor

substrates devices, said semiconductor substrate of one semiconductor device is a silicon substrate, and another of said first and second semiconductor substrate of the other semiconductor device substrates is a compound semiconductor substrate.

Claim 11 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second through-type electrodes and said first and second post electrodes are formed of comprise copper, tungsten, titanium, nickel, aluminum or an alloy thereof.

Claim 12 (Currently Amended): The stacked semiconductor device according to claim 1, wherein a characterized in that gap between said first semiconductor device and said second semiconductor device is filled with an insulating resin.

Claim 13 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second semiconductor devices respectively have the first and second device has, likewise said first semiconductor device, a plurality of post electrodes exposed in surfaces a surface of said first and third insulating [[layer]] layers, and said first and second a plurality of through-type electrodes exposed in surfaces a surface of said second and fourth insulating layers [[layer]], and said first and second through-type electrodes are formed at exposed ends of specified ones of said first and second post electrodes or said first and second through-type

electrodes located in [[the]] an upper surface.

Claim 14 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second post electrodes [[are]] have larger diameter than said first and second through-type electrodes in diameter.

Claim 15 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second circuit elements are active elements and passive elements.

Claim 16 (Currently Amended): The stacked semiconductor device according to claim 1, wherein characterized in that said first and second semiconductor substrates of said respective semiconductor devices have a thickness of around 5 to 50 μm , and said first and third insulating layer has layers have a thickness of around 20 to 100 μm .

Claim 17 (Currently Amended): A semiconductor device comprising characterized by having:

a semiconductor substrate;
circuit elements at a first main surface side of said semiconductor substrate;
a multilayer wiring part on said including a plurality of circuit elements and
configured of a formed at a first main surface side of said semiconductor substrate and

wiring electrically connected with said circuit elements and an insulating layer, the
wiring and the insulating layer being stacked alternately with the insulating layer being
an uppermost layer;

a first insulating layer for covering said insulating layer of said multilayer wiring
part and provided all over said semiconductor substrate, said first insulating layer is a
support member of said semiconductor substrate;

a second insulating layer for covering a second main surface of said
semiconductor substrate that is to become an opposite face against the first main
surface of said semiconductor substrate;

a plurality of post electrodes formed on respective specified said wiring of said
multilayer wiring part and each having a top surface and side surfaces, the top surfaces
to be exposed from [[in]] a surface of said first insulating layer and all the side surfaces
covered by said first insulating layer; and

a plurality of through-type electrodes penetrating from a specified depth of said
multilayer wiring part to a surface of said second insulating layer provided to pierce
through said semiconductor substrate and said second insulating layer from specified
depth of said multilayer wiring part, said through-type electrodes insulated from brought
into contact to said semiconductor substrate through by an insulating film and
connected with said specified wiring of said multilayer wiring part respectively.

Claim 18 (Currently Amended): The semiconductor device according to claim 17,

further comprising characterized in that protruding electrodes are formed at exposed ends of specified ones of said post electrodes and said through-type electrodes.

Claim 19 (Currently Amended): The semiconductor device according to claim 17, wherein characterized in that said post electrodes have [[are]] larger diameter than said through-type electrodes in diameter.

Claim 20 (Currently Amended): The semiconductor device according to claim 17, wherein characterized in that said post electrodes are formed by comprised of a plating film, stud bump electrodes or a CVD film.

Claim 21 (Currently Amended): The semiconductor device according to claim 17, wherein characterized in that said through-type electrodes and said post electrodes are formed comprised of copper, tungsten, titanium, nickel, aluminum or an alloy thereof.

Claim 22 (Currently Amended): The semiconductor device according to claim 17, wherein characterized in that said circuit elements are active elements and passive elements.

Claim 23 (Currently Amended): The semiconductor device according to claim 17, wherein characterized in that said semiconductor substrate has a substrates of said

respective semiconductor devices have thickness of around 5 to 50 μm , and said first insulating layer has thickness of around 20 to 100 μm .

Claims 24 – 46 (Canceled)

Claim 47 (New): A semiconductor device comprising:

a semiconductor substrate having first and second main surfaces, and a circuit on the first main surface;

a multilayer wiring part including an insulating layer and a wiring pattern electrically connected with the circuit, the insulating layer and the wiring pattern disposed over the first main surface alternately with respect to each other;

a first insulating layer on an uppermost layer of said multilayer wiring part;

a second insulating layer over the second main surface;

a first electrode over the first main surface, the first electrode having top and side surfaces and electrically connected with a part of the wiring pattern, the top surface being exposed from a surface of said first insulating layer and all the side surfaces being covered with said first insulating layer; and

a second electrode formed on an inner wall of a through-via which penetrates from the first main surface to the second main surface.

Claim 48 (New): The semiconductor device according to claim 47, wherein said first

insulating layer is thicker than the insulating layer of said multilayer wiring part.

Claim 49 (New): The semiconductor device according to claim 47, wherein said first insulating layer is thicker than said semiconductor substrate.

Claim 50 (New): The semiconductor device according to claim 47, wherein said first insulating layer comprises encapsulation resin.

Claim 51 (New): The semiconductor device according to claim 47, wherein said second electrode is a through-type electrode.